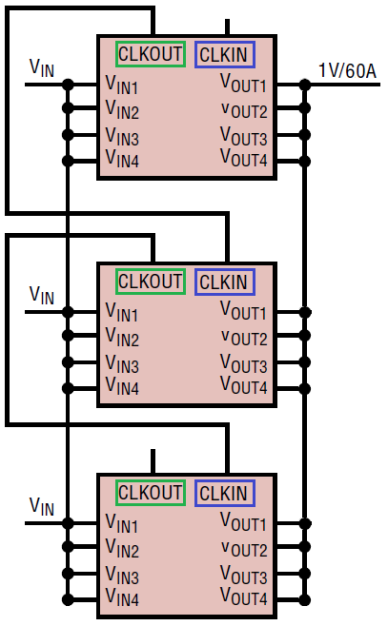
Quad DC/DC Module Regulator with Configurable 5A Output Array

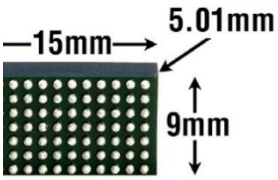
The YPM04644E is a quad DC/DC step-down Power Module regulator with 5A per output. Outputs can be paralleled in an array for up to 20A capability. Included in the package are the switching controllers, power FET, inductors and support components. Operating over an input voltage range of 4V to 18V, or 2.5V to 14V with an external bias supply, the YPM04644 supports an output voltage range of 0.6V to 5.5V. Its high efficiency design delivers 5A continuous output current per channel. Only bulk input and output capacitors are needed.

Multiple Module can be connected in parallel to achieve higher current capability to 60A.

Features

- Quad Output Step-Down Module Regulator
- Wide Input Voltage Range: 4V to 18V
- Output Voltage: 0.6V to 5.5V
- Output Current Each Channel: 5A DC, 7A Peak
- Total Output Voltage Regulation: ±1.5%
- Force CCM, Pulse skip and Burst Mode Operation
- Current Mode Control, Fast Transient Response
- Parallelable for Higher Output Current up to 60A
- Output Voltage Tracking
- Internal Temperature Sensing Diode Output
- External Frequency Synchronization
- Overvoltage, Current and Temperature Protection
- BGA Package 9mm × 15mm × 5.01mm

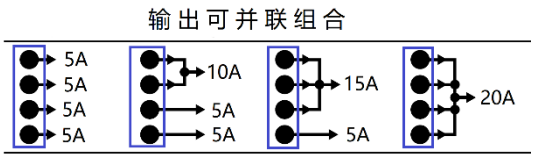


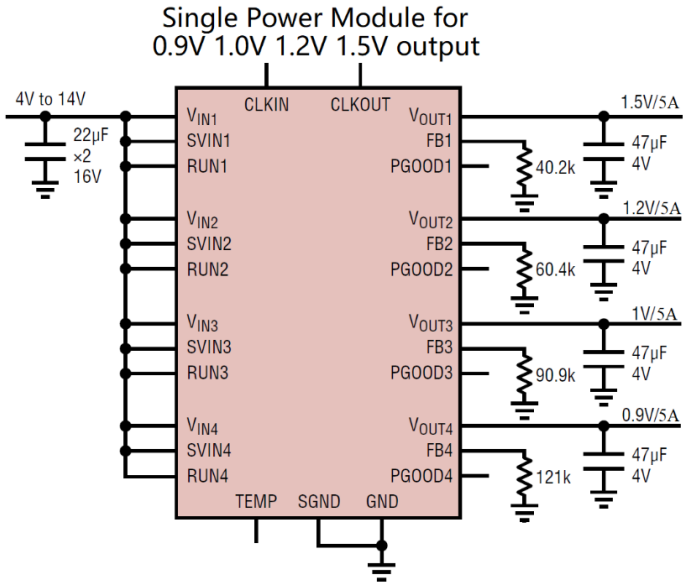


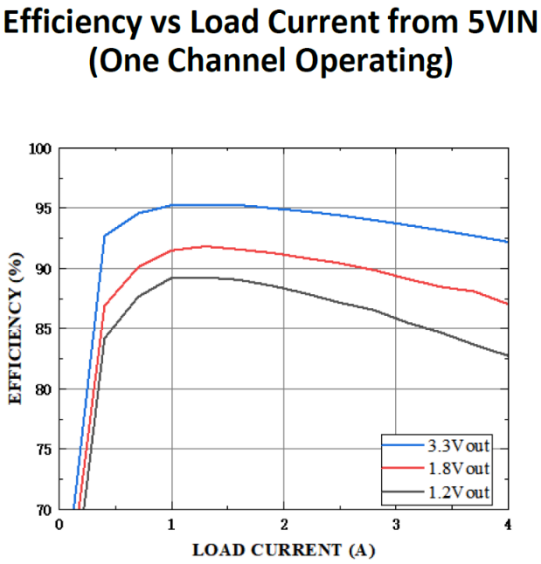
Applications

- Multi-rail Point of Load Regulation
- FPGAs, DSPs and ASICs Applications
- DC Power Distribution

	YPM04644	YPM04644E
Top Feedback Resistor from V_{OUT}-to-V_{FB}	Integrated 60.4k 0.5% Resistor	External (to be added on PCB)
Application	General Applications	To Interface with PMBus power system management supervisory ICs







Absolute Maximum Ratings

Stress in excess of our defined *absolute maximum ratings* may cause permanent damage to the converter. Absolute maximum ratings, also referred to as *non-destructive limits,* are normally tested with one parameter at a time exceeding the limits in the electrical specification.

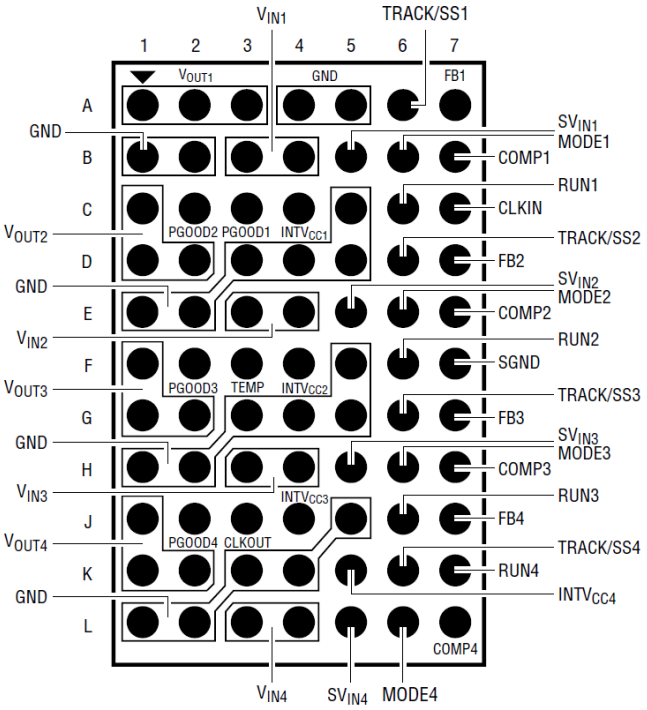
Characteristics	Min	Max	Unit
Operating temperature	-40	125	°C
Storage temperature	-65	150	°C
Peak Solder Reflow Body temperature		245	°C
Input voltage continuous operation	-0.3	15	V
Output Voltage	-0.3	6	V
INTVcc	-0.3	3.6	V
Signal I/O voltage (PGOOD, MODE, TRACK/SS, FB, CLKOUT, CLKIN)	-0.3	INTVcc	V

Pin Description: (YPM04644/YPM04644E)

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A1	V_{OUT1}	B1	GND	C1	V_{OUT2}	D1	V_{OUT2}	E1	GND	F1	V_{OUT3}
A2	V_{OUT1}	B2	GND	C2	PGOOD2	D2	V_{OUT2}	E2	GND	F2	PGOOD3
A3	V_{OUT1}	B3	V_{IN1}	C3	PGOOD1	D3	GND	E3	V_{IN2}	F3	TEMP
A4	GND	B4	V_{IN1}	C4	$INTV_{CC1}$	D4	GND	E4	V_{IN2}	F4	$INTV_{CC2}$
A5	GND	B5	SV_{IN1}	C5	GND	D5	GND	E5	SV_{IN2}	F5	GND
A6	TRACK/SS1	B6	MODE1	C6	RUN1	D6	TRACK/SS2	E6	MODE2	F6	RUN2
A7	FB1	B7	COMP1	C7	CLKIN	D7	FB2	E7	COMP2	F7	SGND

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME		
G1	V_{OUT3}	H1	GND	J1	V_{OUT4}	K1	V_{OUT4}	L1	GND		
G2	V_{OUT3}	H2	GND	J2	PGOOD4	K2	V_{OUT4}	L2	GND		
G3	GND	H3	V_{IN3}	J3	CLKOUT	K3	GND	L3	V_{IN4}		
G4	GND	H4	V_{IN3}	J4	$INTV_{CC3}$	K4	GND	L4	V_{IN4}		
G5	GND	H5	SV_{IN3}	J5	GND	K5	$INTV_{CC4}$	L5	SV_{IN4}		
G6	TRACK/SS3	H6	MODE3	J6	RUN3	K6	TRACK/SS4	L6	MODE4		
G7	FB3	H7	COMP3	J7	FB4	K7	RUN4	L7	COMP4		

TOP VIEW

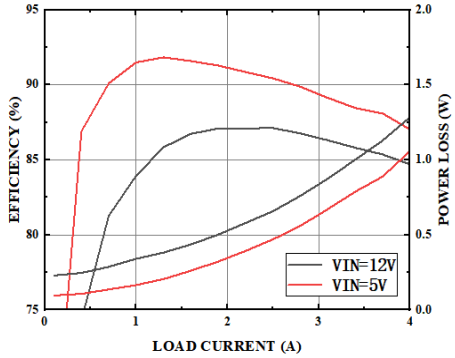


Electrical characteristics

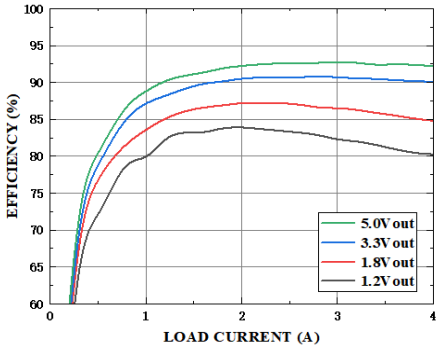
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}, SV_{IN}	Input DC Voltage	$SV_{IN} = V_{IN}$	4		18	V
$V_{OUT(RANGE)}$	Output Voltage Range		0.6		5.5	V
$V_{OUT(DC)}$	Total Variation with Line and Load	C_{IN} = 22µF, C_{OUT} = 100µF Ceramic, MODE = $INTV_{CC}$, V_{IN} = 4V to 14V, I_{OUT} = 0A to 5A, V_{OUT} = 1.5V	1.477	1.50	1.523	V
V_{RUN}	RUN Pin ON Threshold	V_{RUN} Rising	1.1	1.2	1.3	V
$I_{Q(SVIN)}$	Input Supply Bias Current	V_{IN} = 12V, V_{OUT} = 1.8V, MODE = $INTV_{CC}$		18.8		mA
		V_{IN} = 12V, V_{OUT} = 1.8V, MODE = GND		1.14		mA
		Shutdown, RUN = 0, V_{IN} = 12V		0.10		mA
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 5A		0.695		A
$I_{OUT(DC)}$	Output Continuous Current Range	V_{IN} = 12V, V_{OUT} = 1.5V	0		4	A
ΔV_{OUT} (Line)/V_{OUT}	Line Regulation Accuracy	V_{OUT} = 1.5V, V_{IN} = 4V to 14V, I_{OUT} = 0A		0.04	0.15	%/V
ΔV_{OUT} (Load)/V_{OUT}	Load Regulation Accuracy	V_{OUT} = 1.5V, I_{OUT} = 0A to 5A		0.5	1	%
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 94µF Ceramic, V_{IN} = 12V, V_{OUT} = 1.8V		5.83		mV
$\Delta V_{OUT(START)}$	Turn-On Overshoot	I_{OUT} = 0A, C_{OUT} = 94µF Ceramic, V_{IN} = 12V, V_{OUT} = 1.8V		53.3		mV
t_{START}	Turn-On Time	C_{OUT} = 94µF, No Load, TRACK/SS = 0.1µF, V_{IN} = 12V, V_{OUT} = 1.8V		6.2		ms
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 94µF, V_{IN} = 12V, V_{OUT} = 1.8V		43.3		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 94µF, V_{IN} = 12V, V_{OUT} = 1.8V		70		µs
I_{OUTPK}	Output Current Limit	V_{IN} = 12V, V_{OUT} = 1.8V	6.7	7		A
V_{FB}	Voltage at FB Pin	I_{OUT} = 0A, V_{OUT} = 1.5V, 0°C to 125°C	0.594	0.60	0.606	V
		I_{OUT} = 0A, V_{OUT} = 1.5V, –40°C to 125°C	0.592	0.6	0.608	V
I_{FB}	Current at FB Pin				±30	nA
R_{FBHI}	Resistor Between V_{OUT} and FB Pins	YPM04644 Only	60.05	60.40	60.75	kΩ
$I_{TRACK/SS}$	Track Pin Soft-Start Pull-Up Current	TRACK/SS = 0V		2.5	4	µA
$V_{IN(UVLO)}$	V_{IN} Undervoltage Lockout	V_{IN} Falling	2.4	2.6	2.8	V
		V_{IN} Hysteresis		350		mV
$t_{ON(MIN)}$	Minimum On-Time			40		ns
$t_{OFF(MIN)}$	Minimum Off-Time			70		ns
V_{PGOOD}	PGOOD Trip Level	V_{FB} With Respect to Set Output V_{FB} Ramping Negative	–13	-10	-7	%
		V_{FB} Ramping Positive	7	10	13	%
I_{PGOOD}	PGOOD Leakage				2	µA
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 1mA		0.02	0.1	V
V_{INTVCC}	Internal V_{CC} Voltage	SV_{IN} = 4.5V to 14V	4.243	4.248	4.250	V
V_{INTVCC} Load Reg	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 20mA		0.5		%
f_{OSC}	Oscillator Frequency			1		MHz
CLKIN	CLKIN Threshold			0.7		V

TYPICAL PERFORMANCE CHARACTERISTICS

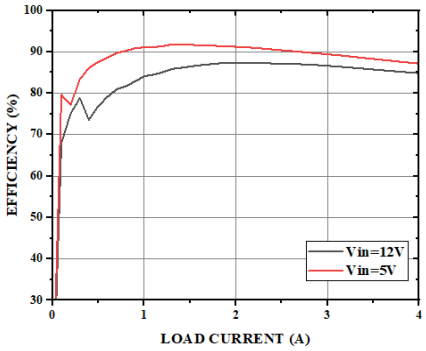
1.8V Output Efficiency and Power Loss



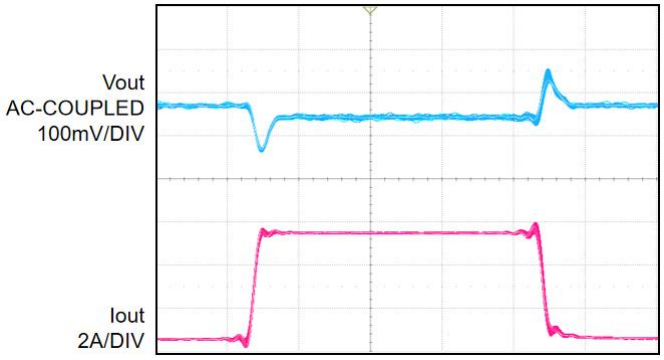
Efficiency vs Load Current from $12V_{IN}$



DCM Mode Efficiency from $1.5V_{OUT}$

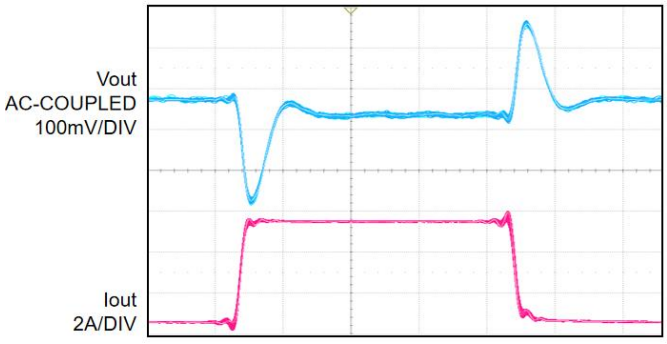


1.2V Output Transient Response



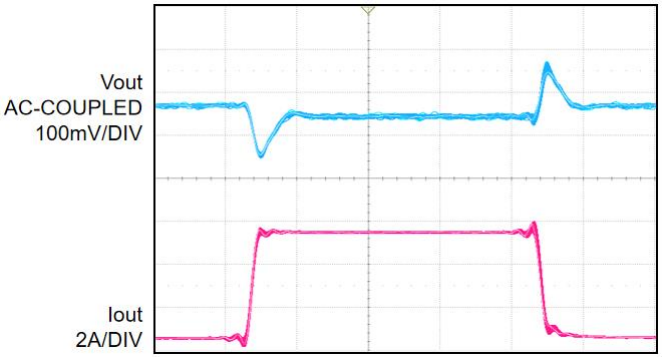
V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 0A to 5A, 0.33A/µs Output Capacitor = 94µF

3.3V Output Transient Response



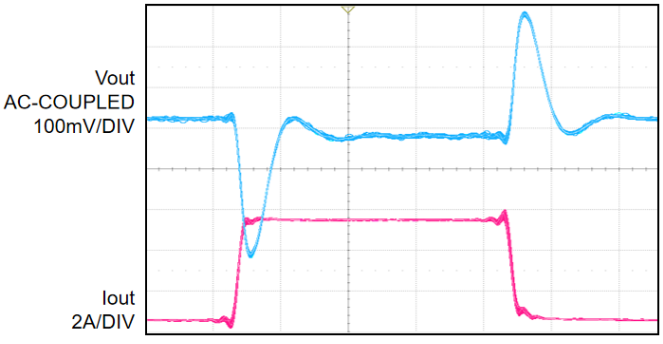
V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A to 5A, 0.33A/µs Output Capacitor = 94µF

1.8V Output Transient Response



V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 0A to 5A, 0.33A/µs Output Capacitor = 94µF

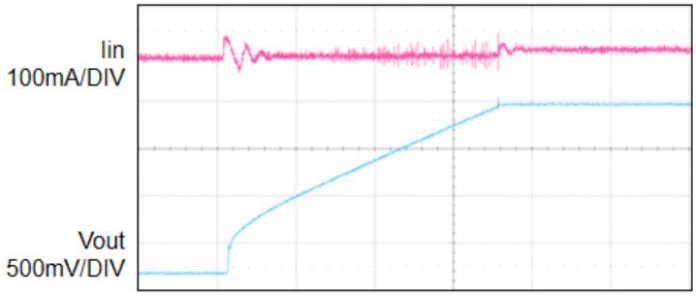
5.0V Output Transient Response



V_{IN} = 12V, V_{OUT} = 5.0V, I_{OUT} = 0A to 5A, 0.33A/µs Output Capacitor = 94µF

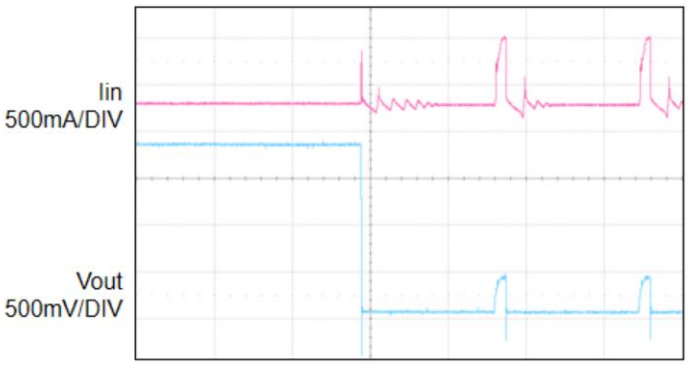
TYPICAL PERFORMANCE CHARACTERISTICS

Start-Up with No Load



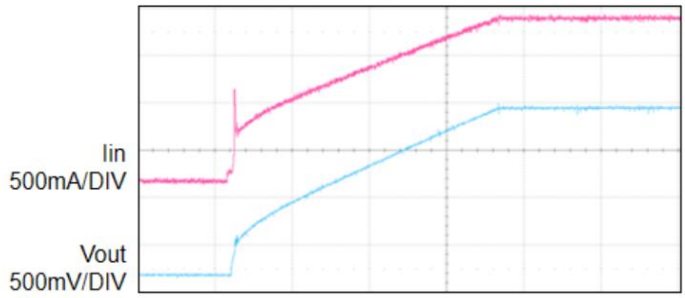
V_{IN} = 12V, V_{OUT} =1.8V, Input Capacitor = 330µF

Short-Circuit with No Load



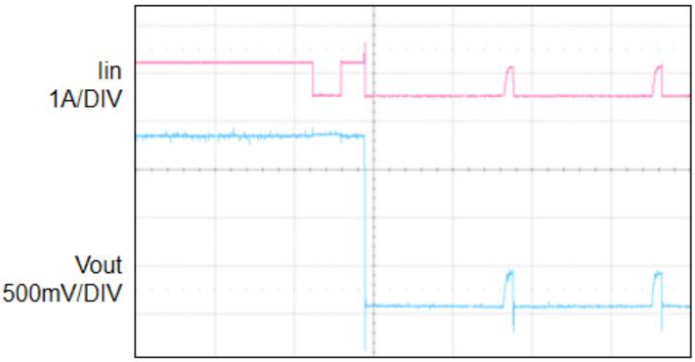
V_{IN} = 12V, V_{OUT} =1.8V, Input Capacitor = 330µF, Output Capacitor = 94µF

Start-Up with 4A Load



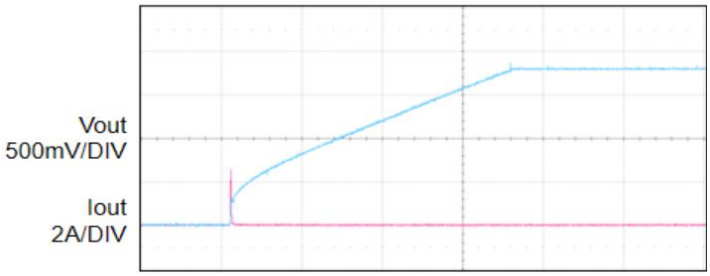
V_{IN} = 12V, V_{OUT} =1.8V, Input Capacitor = 330µF

Short-Circuit with 4A Load



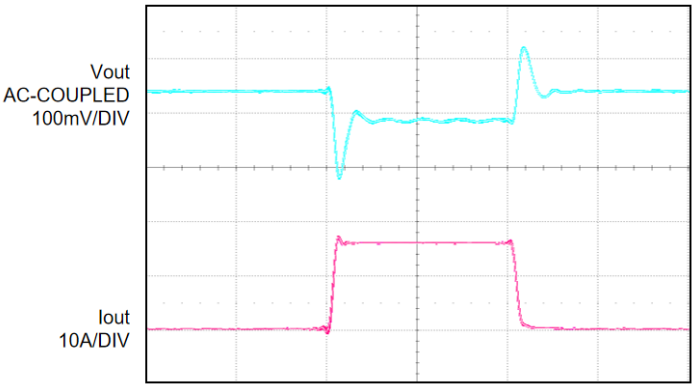
V_{IN} = 12V, V_{OUT} =1.8V, Input Capacitor = 330µF, Output Capacitor = 94µF

Recovery to No Load from Short-Circuit



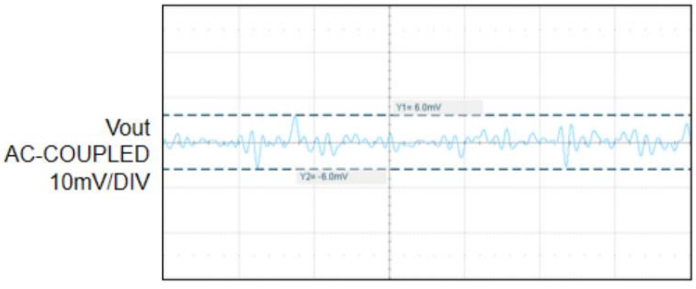
V_{IN} = 12V, V_{OUT} =1.8V, Input Capacitor = 330µF, Output Capacitor = 94µF

1.8V Output Transient Response (4-Channel Paralleled)



V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 0A to 16A, 1A/µs, Output Capacitor =4X94µF=376uF

Output Ripple



V_{IN} = 12V, V_{OUT} =1.8V, Input Capacitor = 330µF, Output Capacitor = 94µF

PIN FUNCTIONS *(PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG Module PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.)*

V_{OUT1} (A1, A2, A3), V_{OUT2} (C1, D1, D2), V_{OUT3} (F1, G1, G2), V_{OUT4} (J1, K1, K2): Power Output Pins of Each Switching Mode Regulator Channel. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. See the Applications Information section for paralleling outputs.

GND (A4-A5, B1-B2, C5, D3-D5, E1-E2, F5, G3-G5, H1-H2, J5, K3-K4, L1-L2): Power Ground Pins for Both Input and Output Returns. Use large PCB copper areas to connect all GND together.

V_{IN1} (B3, B4), V_{IN2} (E3, E4), V_{IN3} (H3, H4), V_{IN4} (L3, L4): Power input pins connect to the drain of the internal top MOSFET for each switching mode regulator channel. Apply input voltages between these pins and GND pins. Recommend placing input decoupling capacitance directly between each of VIN pins and GND pins.

PGOOD1, PGOOD2, PGOOD3, PGOOD4 (C3, C2, F2, J2): Output Power Good with Open-Drain Logic of Each Switching Mode Regulator Channel. PGOOD is pulled to ground when the voltage on the FB pin is not within ±10% of the internal 0.6V reference.

CLKOUT (J3): Output Clock Signal for Parallel Operation of the Module. The phase of CLKOUT with respect to CLKIN is set to 180°. CLKOUT's peak-to-peak amplitude is INTVCC to GND. See the Application Information section for details. Strictly output; do not drive this pin. CLKOUT is only active when RUN4 is enabled.

$INTV_{CC1}$, $INTV_{CC2}$, $INTV_{CC3}$, $INTV_{CC4}$ (C4, F4, J4, K5): Internal 3.3V Regulator Output of Each Switching Mode Regulator Channel. The internal power drivers and control circuits are powered from this voltage. Each pin is internally decoupled to GND with 1μF low ESR ceramic capacitor already.

SV_{IN1}, SV_{IN2}, SV_{IN3}, SV_{IN4} (B5, E5, H5, L5): Signal VIN Filtered input voltage to the internal 3.3V regulator for the control circuitry of each Switching mode Regulator Channel. Tie this pin to the VIN pin respectively in most applications. Connect SVIN to an external voltage supply of at least 4V which must also be greater than VOUT.

TRACK/SS1, TRACK/SS2, TRACK/SS3, TRACK/SS4 (A6, D6, G6, K6): Output Tracking and Soft-Start Pin of Each Switching Mode Regulator Channel. Allows the user to control the rise time of the output voltage. Putting a voltage below 0.6V on this pin bypasses the internal reference input to the error amplifier, instead it servos the FB pin to match the TRACK voltage. Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. There's an internal 2.5μA pull-up current from INTVCC on this pin, so putting a capacitor here provides soft-start function.

MODE1, MODE2, MODE3, MODE4 (B6, E6, H6, L6): Operation Mode Select for Each Switching Mode Regulator Channel. Tie this pin to INTVCC to force continuous synchronous operation at all output loads. Tying it to SGND enables discontinuous current mode operation at light loads. Do not leave floating.

RUN1, RUN2, RUN3, RUN4 (C6, F6, J6, K7): Run Control Input of Each Switching Mode Regulator Channel. Enable regulator operation by tying the specific RUN pin above 1.2V. Pulling it below 1.1V shuts down the respective regulator channel. Do not leave floating.

FB1, FB2, FB3, FB4 (A7, D7, G7, J7): The Negative Input of the Error Amplifier for Each Switching Mode Regulator Channel. Internally, in YPM04644, this pin is connected to VOUT of each channel with a 60.4kΩ precision resistor. Different output voltages can be programmed with an additional resistor between the FB and GND pins for the YPM04644, and two resistors between the VOUT, FB and GND pins for the YPM04644E. In Parallel operation, tying the FB pins together allows for parallel operation. See the Applications Information section for details.

COMP1, COMP2, COMP3, COMP4 (B7, E7, H7, L7): Current Control Threshold and Error Amplifier Compensation Point of Each Switching Mode Regulator Channel. The internal current comparator threshold is proportional to this voltage. Tie the COMP pins together for parallel operation. The device is internally compensated.

CLKIN (C7): External Synchronization Input to Phase Detector of the Module. This pin is internally terminated to SGND with 20kΩ. The phase-locked loop will force the channel 1 turn-on signal to be synchronized with the rising edge of the CLKIN signal. Channel 2, channel 3 and channel 4 will also be synchronized with the rising edge of the CLKIN signal with a pre-determined phase shift. See the Applications Information section for details.

SGND (F7): Signal Ground Connection. SGND is connected to GND internally through single point. Use a separated SGND ground copper area for the ground of the feedback resistor and other components connected to signal pins. A second connection between the PGND plane and SGND plane is recommended on the backside of the PCB underneath the module.

TEMP (F3): Onboard Temperature Diode for Monitoring the VBE Junction Voltage Change with Temperature.

DECOUPLING REQUIREMENTS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement (V_{IN} = 4V to 14V, V_{OUT} = 1.5V)	I_{OUT} = 5A	4.7	10		μF
C_{OUT}	External Output Capacitor Requirement (V_{IN} = 4V to 14V, V_{OUT} = 1.5V)	I_{OUT} = 5A	22	47		μF

OPERATION

The YPM04644 is a quad output standalone non-isolated switch mode DC/DC power module. It has four separate regulator channels with each of them capable of delivering up to 5A continuous output current with few external input and output capacitors. Each regulator provides precisely regulated output voltage programmable from 0.6V to 5.5V via a single external resistor (two resistors for YPM04644E) over 4V to 14V input voltage range. With an external bias voltage, this module can operate from an input voltage as low as 2.375V.

The YPM04644 integrates four separate constant frequency controlled on-time valley current mode regulators, power MOSFETs, inductors, and other supporting discrete components. The typical switching frequency is set to 1MHz. For switching noise-sensitive applications, the regulator can be externally synchronized to a clock from 700kHz to 1.3MHz.

With current mode control and internal feedback loop compensation, the YPM04644 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

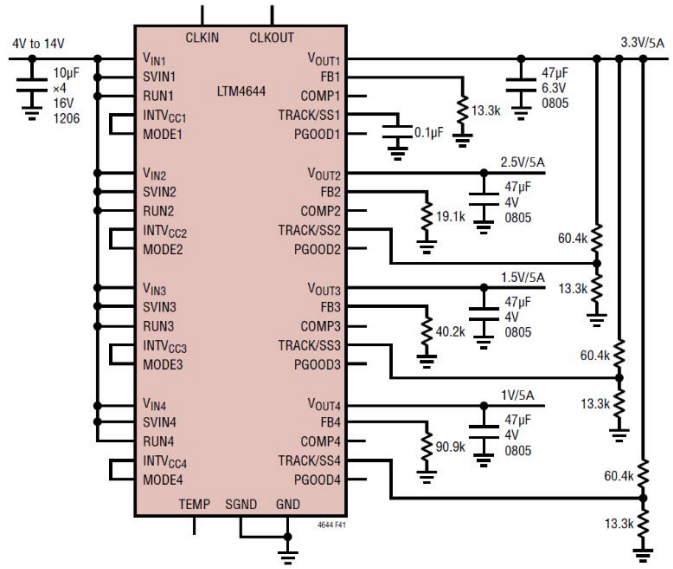
Current mode control provides the flexibility of paralleling any of the separate regulator channels with accurate current sharing. With a built-in clock interleaving between each two regulator channels, the YPM04644 could easily employ a 2+2, 3+1 or 4 channels parallel operation which is more than flexible in a multi-rail POL application like FPGA. Furthermore, the YPM04644 has CLKIN and CLKOUT pins for frequency synchronization or paralleling multiple devices which allow up to 8 phases cascaded to run simultaneously.

Current mode control also provides cycle-by-cycle fast current monitoring. Foldback current limiting is provided in an overcurrent condition to reduce the inductor valley current to approximately 40% of the original value when V_{FB} drops. An internal overvoltage and undervoltage comparators pull the open-drain PGOOD output low if the output feedback voltage exits a ±10% window around the regulation point. Continuous conduction mode (CCM) operation is forced during OV and UV conditions except during start-up when the TRACK pin is ramping up to 0.6V.

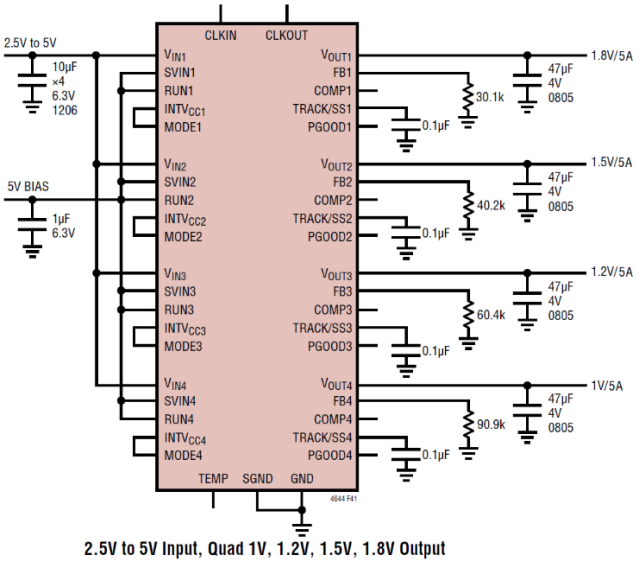
Pulling the RUN pin below 1.1V forces the controller into its shutdown state, turning off both power MOSFETs and most of the internal control circuitry. At light load currents, discontinuous conduction mode (DCM) operation can be enabled to achieve higher efficiency compared to continuous conduction mode (CCM) by setting the MODE pin to SGND. The TRACK/SS pin is used for power supply tracking and soft-start programming.

A temperature diode is included inside the module to monitor the temperature of the module.

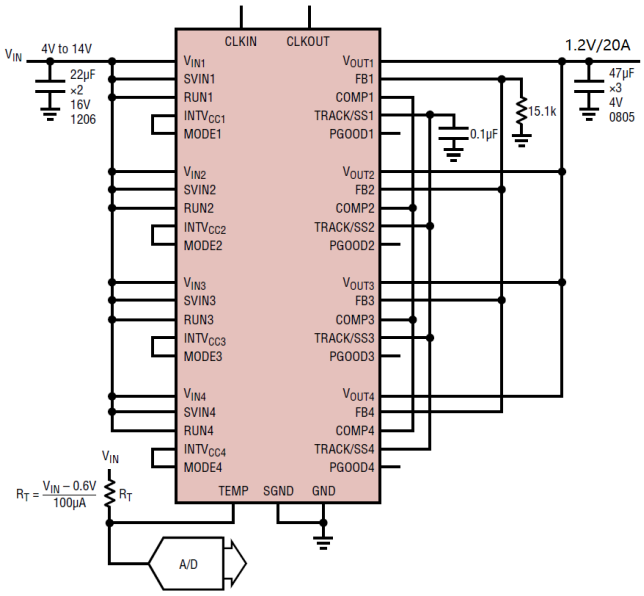
TYPICAL APPLICATIONS INFORMATION



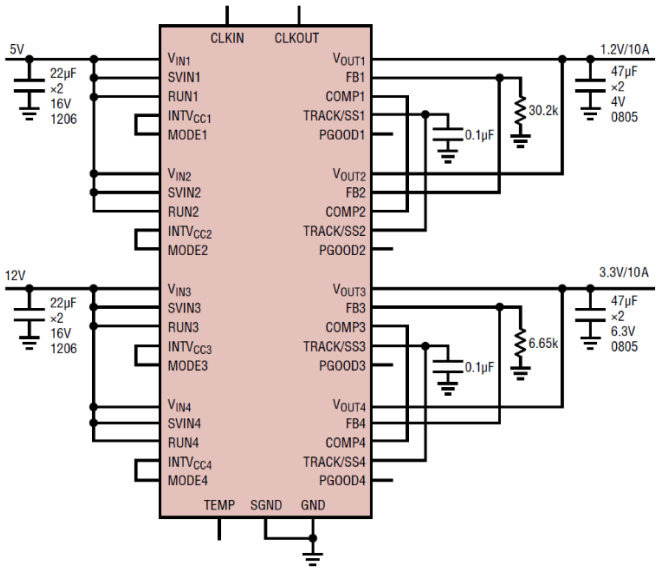
4V to 14V Input, Quad 1.2V, 1.5V, 2.5V and 3.3V Output with Tracking



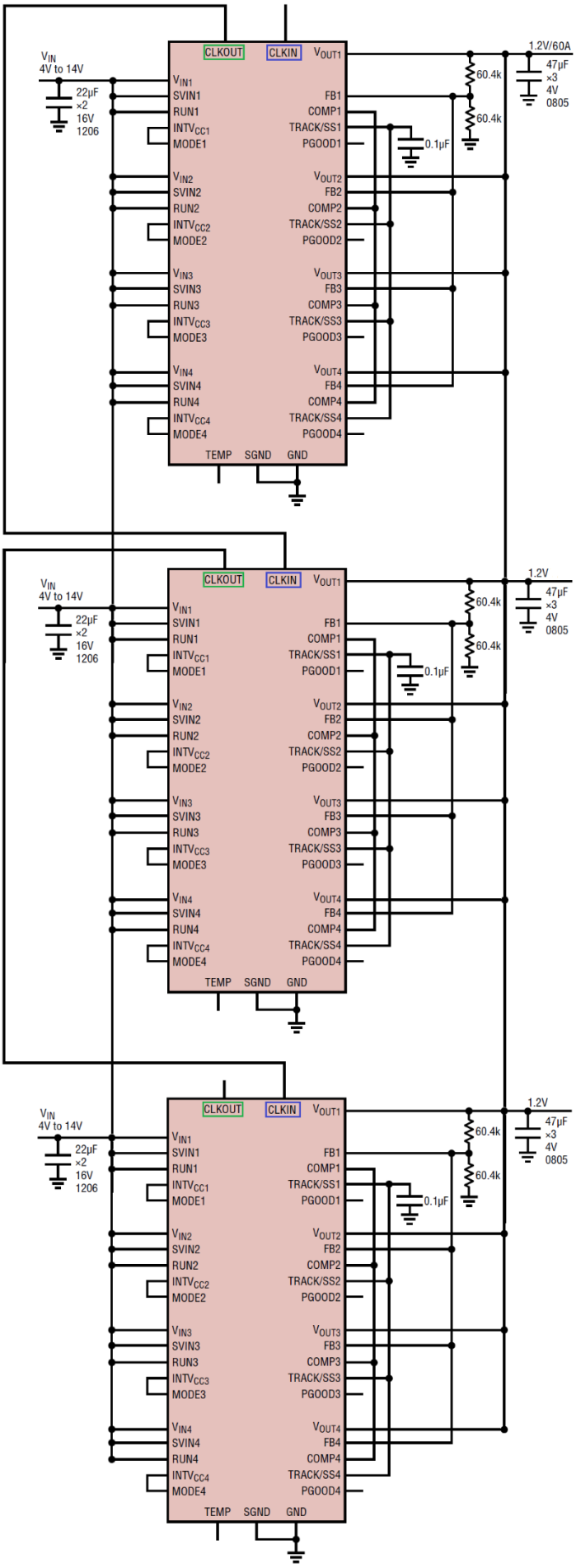
2.5V to 5V Input, Quad 1V, 1.2V, 1.5V, 1.8V Output



4V to 14V Input, 4-Phase, 1.2V at 20A Design with Temperature Monitoring



12V and 5V Two Separate Input, 1.2V and 3.3V at 10A Output


VIN
4V to 14V
22µF
×2
16V
1206
CLKOUT
CLKIN
VIN1
SVIN1
RUN1
INTVCC1
MODE1
VIN2
SVIN2
RUN2
INTVCC2
MODE2
VIN3
SVIN3
RUN3
INTVCC3
MODE3
VIN4
SVIN4
RUN4
INTVCC4
MODE4
TEMP
SGND
GND
VOUT1
FB1
COMP1
TRACK/SS1
PGOOD1
VOUT2
FB2
COMP2
TRACK/SS2
PGOOD2
VOUT3
FB3
COMP3
TRACK/SS3
PGOOD3
VOUT4
FB4
COMP4
TRACK/SS4
PGOOD4
60.4k
60.4k
0.1µF
1.2V/60A
47µF
×3
4V
0805
1.2V
47µF
×3
4V
0805

The typical YPM04644 application circuit is shown as above. External component selection is primarily determined by the input voltage, the output voltage and the maximum load current.

VIN to VOUT Step-Down Ratios

There are restrictions in the maximum VIN and VOUT stepdown ratio that can be achieved for a given input voltage due to the minimum off-time and minimum on-time limits of each regulator. The minimum off-time limit imposes a maximum duty cycle which can be calculated as: $D_{max} = 1 - t_{off(min)} \cdot f_{sw}$ where $t_{OFF(MIN)}$ is the minimum off-time, 70ns typical for YPM04644, and f_{SW} is the switching frequency. Conversely the minimum on-time limit imposes a minimum duty cycle of the converter which can be calculated as: $D_{min} = t_{on(min)} \cdot f_{sw}$ where $t_{ON(MIN)}$ is the minimum on-time, 40ns typical for YPM04644. In the rare cases where the minimum duty cycle is surpassed, the output voltage will still remain in regulation, but the switching frequency will decrease from its programmed value. Note that additional thermal derating may be applied.

Output Voltage Programming (YPM04644)

The PWM controller has an internal 0.6V reference voltage. As shown in the Block Diagram, a 60.4k internal feedback resistor connects each regulator channel from V_{OUT} pin to FB pin. Adding a resistor $R_{FB(BOT)}$ from FB pin to GND programs the output voltage: $R_{FB(BOT)} = \frac{60.4k}{\frac{V_{out}}{0.6}-1}$

Table1.VFB Resistor Table vs Various Output Voltages

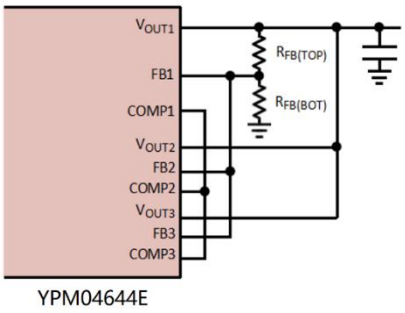
V_{OUT} (V)	0.6	1.0	1.2	1.5	1.8	2.5	3.3	5.0
$R_{FB(BOT)}$ (k)	Open	90.9	60.4	40.2	30.1	19.1	13.3	8.25

For parallel operation of N channels, use the following equation can be used to solve for $R_{FB(BOT)}$. Tie the V_{OUT} and the FB and COMP pins together for each paralleled output with a single resistor to GND as determined by: $R_{FB(BOT)} = \frac{\frac{60.4k}{N}}{\frac{V_{out}}{0.6}-1}$

OUTPUT VOLTAGE PROGRAMMING (YPM04644E)

The PWM controller has an internal 0.6V reference voltage. Adding two resistors $R_{FB(TOP)}$ from V_{OUT} to FB pin and $R_{FB(BOT)}$ from FB pin to GND programs the output voltage: $R_{FB(BOT)} = \frac{R_{FB(TOP)}}{\frac{V_{out}}{0.6}-1}$

For parallel operation of N Channels, only one set of $R_{FB(TOP)}$ and $R_{FB(BOT)}$ is needed while tying the V_{OUT}, FB and COMP pins from different channels together.



	YPM04644	YPM04644E
Top Feedback Resistor from V_{OUT}-to-V_{FB}	Integrated 60.4k 0.5% Resistor	External (to be added on PCB)
Application	General Applications	To Interface with PMBus power system management

Input Decoupling Capacitors

The YPM04644 module should be connected to a low ac-impedance DC source. For each regulator channel, a 10μF input ceramic capacitor is recommended for RMS ripple current decoupling. A bulk input capacitor is only needed when the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. The bulk capacitor can be an electrolytic aluminum capacitor or polymer capacitor.

Without considering the inductor ripple current, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{out(max)}}{\eta\%} \cdot \sqrt{D \cdot (1-D)}$$

where $\eta\%$ is the estimated efficiency of the power module.

Output Decoupling Capacitors

With an optimized high frequency, high bandwidth design, only single piece of low ESR output ceramic capacitor is required for each regulator channel to achieve low output voltage ripple and very good transient response. Additional output filtering may be required by the system designer, if further reduction of output ripples or dynamic transient spikes is required.

Multiphase operation will reduce effective output ripple as a function of the number of phases, but the output capacitance will be more a function of stability and transient response.

Discontinuous Conduction Mode (DCM)

In applications where low output ripple and high efficiency at intermediate current are desired, discontinuous conduction mode (DCM) should be used by connecting the MODE pin to SGND. At light loads the internal current comparator may remain tripped for several cycles and force the top MOSFET to stay off for several cycles, thus skipping cycles. The inductor current does not reverse in this mode

Force Continuous Conduction Mode (CCM)

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous conduction mode operation should be used. Forced continuous operation can be enabled by tying the MODE pin to INTVCC. In this mode, inductor current is allowed to reverse during low output loads, the COMP voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the YPM04644's output voltage is in regulation.

Operating Frequency

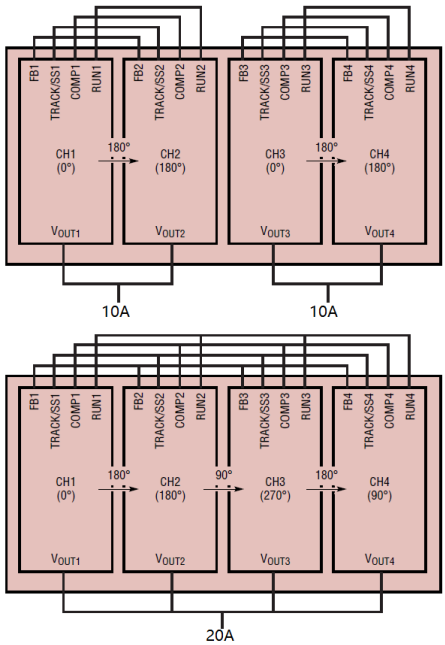
The operating frequency of the YPM04644 is optimized to achieve the compact package size and the minimum output ripple voltage while still keeping high efficiency. The default operating frequency is internally set to 1MHz. In most applications, no additional frequency adjusting is required. If any operating frequency other than 1MHz is required by application, the Module regulator can be externally synchronized to a clock from 700kHz to 1.3MHz.

Frequency Synchronization and Clock In

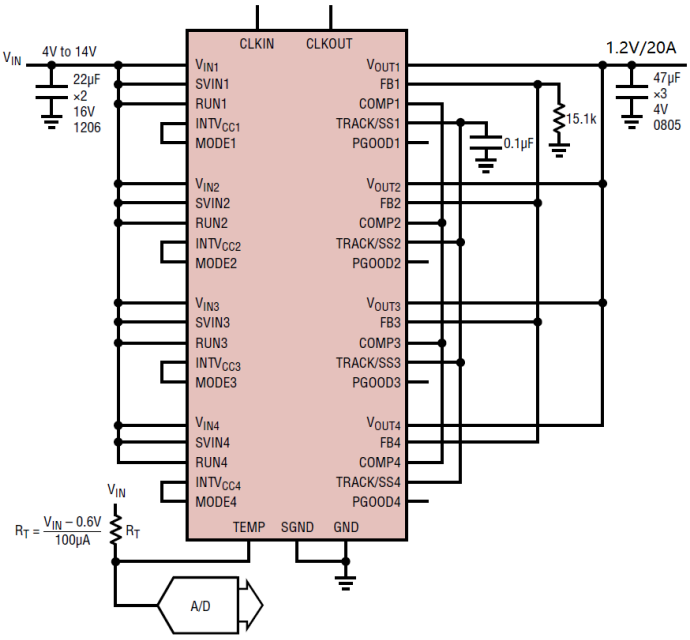
The power module has a phase-locked loop comprised of an internal voltage-controlled oscillator and a phase detector. This allows all internal top MOSFET turn-on to be locked to the rising edge of the same external clock. The external clock frequency range must be within ±30% around the 1MHz set frequency. A pulse detection circuit is used to detect a clock on the CLKIN pin to turn on the phase-locked loop. The pulse width of the clock has to be at least 400ns. The clock high level must be above 2V and clock low level below 0.3V. During the start-up of the regulator, the phase-locked loop function is disabled.

Multichannel Parallel Operation

For loads that demand more than 5A of output current, the YPM04644 multiple regulator channels can be easily paralleled to provide more output current without increasing input and output voltage ripples. The YPM04644 has preset built-in phase shift between each two of the four regulator channels which is suitable to employ a 2+2, 3+1 or 4 channels parallel operation.



2+2 and a 4-channels parallel schematic for clock phasing



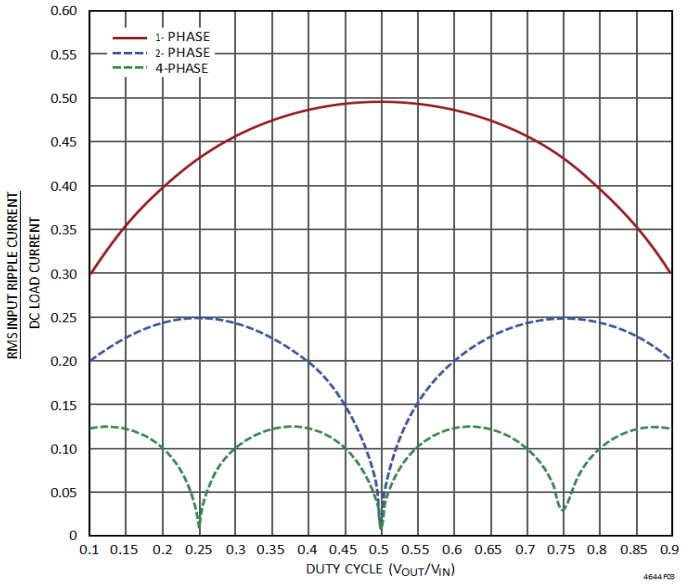
4V to 14V Input, 4-Phase, 1.2V at 20A Design with Temperature Monitoring

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used when all of the outputs are tied together to achieve a single high output current design.

The YPM04644 device is an inherently current-mode-controlled device, so parallel modules will have very good current sharing. This will balance the thermals on the design. Please tie the RUN, TRACK/SS, FB and COMP pins of each paralleling channel together.

Input RMS Ripple Current Cancellation

Below graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases.



Normalized RMS Ripple Current for Single Phase or Polyphase Applications

Soft-Start and Output Voltage Tracking

The TRACK/SS pin provides a means to either soft-start of each regulator channel or track it to a different power supply. A capacitor on the TRACK/SS pin will program the ramp rate of the output voltage. An internal 2.5μA current source will charge up the external soft-start capacitor towards the INTVCC voltage. When the TRACK/SS voltage is below 0.6V, it will take over the internal 0.6V reference voltage to control the output voltage. The total soft-start time can be calculated as:

$$t_{ss} = 0.6 \cdot \frac{C_{ss}}{2.5\mu A}$$ where CSS is the capacitance on the TRACK/SS pin. Current fold back and forced continuous mode are disabled during the soft-start process.

Output voltage tracking can also be programmed externally using the TRACK/SS pin of each regulator channel. The output can be tracked up and down with another regulator. Figure 4 and Figure 5 show an example waveform and schematic of a ratio-metric tracking where the slave regulator's (V_{OUT2}, V_{OUT3} and V_{OUT4}) output slew rate is proportional to the master's (V_{OUT1}).

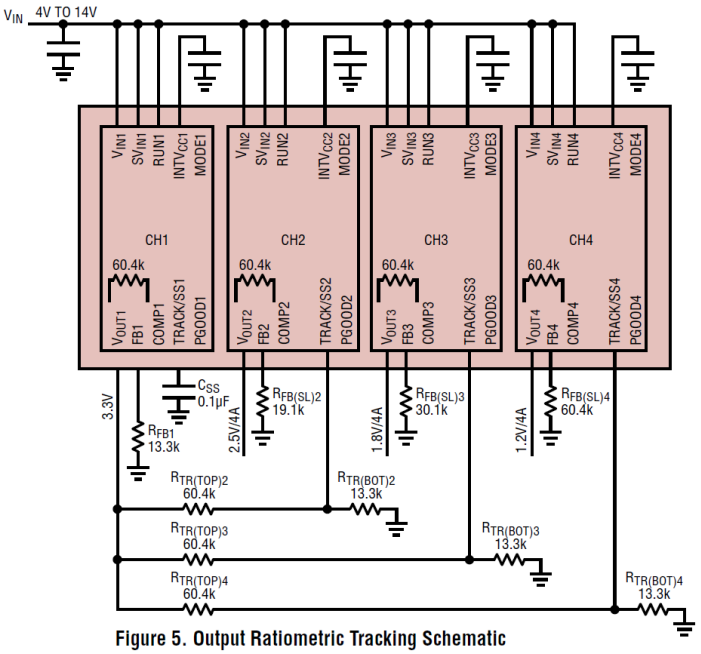


Figure 5. Output Ratiometric Tracking Schematic

Since the slave regulator's TRACK/SS is connected to the master's output through a $R_{TR(TOP)}/R_{TR(BOT)}$ resistor divider and its voltage used to regulate the slave output voltage when TRACK/SS voltage is below 0.6V, the slave output voltage and the master output voltage should satisfy the following equation during the start-up.

$$V_{out(SL)} \cdot \frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k} = V_{out(MA)} \cdot \frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}$$

Where the 60.4k is the integrated top feedback resistor and the $R_{FB(SL)}$ is the external bottom feedback resistor of the YPM04644. The $R_{TR(TOP)}/R_{TR(BOT)}$ is the resistor divider on the TRACK/SS pin of the slave regulator, as shown in Figure 5. Following the upper equation, the master's output slew rate (MR) and the slave's output slew rate (SR) in volts/time is determined by: $\frac{MR}{SR} = \frac{\frac{R_{FB(SL)}}{R_{FB(SL)}+60.4k}}{\frac{R_{TR(BOT)}}{R_{TR(TOP)}+R_{TR(BOT)}}}$

For example, $V_{OUT(MA)}$ = 3.3V, MR = 3.3V/24ms and $V_{OUT(SL)}$ = 1.2V, SR = 1.2V/24ms as V_{OUT1} and V_{OUT4} shown in Figure 5. From the equation, we could solve out that $R_{TR4(TOP)}$ = 60.4k and $R_{TR4(BOT)}$ = 13.3k is a good combination. Follow the same equation, we can get the same $R_{TR(TOP)}/R_{TR(BOT)}$ resistor divider value for V_{OUT2} and V_{OUT3}.

The TRACK pins will have the 2.5μA current source on when a resistive divider is used to implement tracking on that specific channel. This will impose an offset on the TRACK pin input. Smaller value resistors with the same ratios as the resistor values calculated from the above equation can be used. For example, where the 60.4k is used then a 6.04k can be used to reduce the TRACK pin offset to a negligible value.

The coincident output tracking can be recognized as a special ratio metric output tracking which the master's output slew rate (MR) is the same as the slave's output slew rate (SR), as waveform shown in Figure 6.

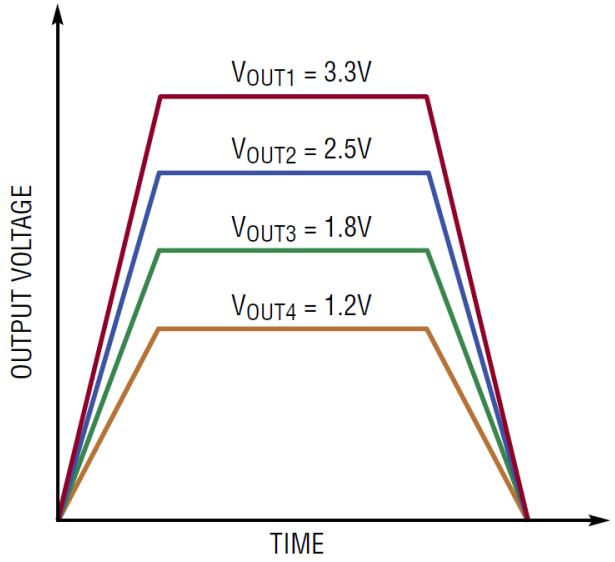


Figure 4. Output Ratiometric Tracking Waveform

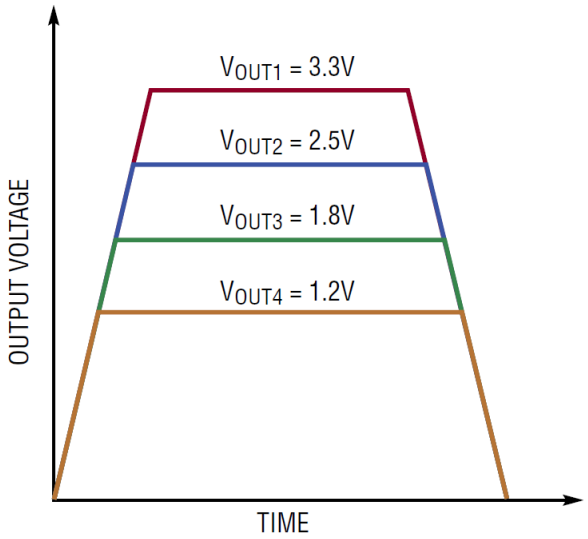


Figure 6. Output Coincident Tracking Waveform

From the equation we could easily find out that, in the coincident tracking, the slave regulator's TRACK/SS pin resistor divider is always the same as its output voltage divider.

$$\frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k} = \frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}$$

For example, $R_{TR4(TOP)}$ = 60.4k and $R_{TR4(BOT)}$ = 60.4k is a good combination for coincident tracking for $V_{OUT(MA)}$ = 3.3V and $V_{OUT(SL)}$ = 1.2V application.

Power Good

The PGOOD pins are open drain pins that can be used to monitor each valid output voltage regulation. This pin monitors a ±10% window around the regulation point. A resistor can be pulled up to a particular supply voltage for monitoring. To prevent unwanted PGOOD glitches during transients or dynamic V_{OUT} changes, the YPM04644's PGOOD falling edge includes a blanking delay of approximately 52 switching cycles.

Stability Compensation

The YPM04644 module internal compensation loop of each regulator channel is designed and optimized for low ESR ceramic output capacitors only application. In case of bulk output capacitors is required for output ripples or dynamic transient spike reduction, an additional 10pF to 15pF phase boost capacitor is required between the V_{OUT} and FB pins.

RUN Enable

Pulling the RUN pin of each regulator channel to ground forces the regulator into its shutdown state, turning off both power MOSFETs and most of its internal control circuitry. Bringing the RUN pin above 0.7V turns on the internal reference only, while still keeping the power MOSFETs off. Further increasing the RUN pin voltage above 1.2V will turn on the entire regulator channel.

Pre-Biased Output Start-Up

There may be situations that require the power supply to start up with some charge on the output capacitors. The YPM04644 can safely power up into a pre-biased output without discharging it. The YPM04644 accomplishes this by forcing discontinuous mode (DCM) operation until the TRACK/SS pin voltage reaches 0.6V reference voltage. This will prevent the BG from turning on during the pre-biased output start-up which would discharge the output.

Do not pre-bias YPM04644/YPM4644E with an output voltage higher than INTVCC (3.3V).

Overtemperature Protection

The internal overtemperature protection monitors the junction temperature of the module. If the junction temperature reaches approximately 160°C, both power switches will be turned off until the temperature drops about 15°C cooler.

Low Input Application

The YPM04644 module has a separate SV_{IN} pin for each regulator channel which makes it compatible with operation from an input voltage as low as 2.375V. The SV_{IN} pin is the signal input of the regulator control circuitry while the V_{IN} pin is the power input which directly connected to the drain of the top MOSFET. In most application with input voltage ranges from 4V to 14V, connect the SV_{IN} pin directly to the V_{IN} pin of each regulator channel. An optional filter, consisting of a resistor (1Ω to 10Ω) between SV_{IN} and V_{IN} ground, can be placed for additional noise immunity. This filter is not necessary in most cases if good PCB layout practices are followed. In a low input voltage (2.375V to 4V) application, or to reduce power dissipation by the internal bias LDO, connect SV_{IN} to an external voltage higher than 4V with a 0.1μF local bypass capacitor. Please note, SV_{IN} voltage cannot go below V_{OUT} voltage.

Temperature Monitoring

A diode connected PNP transistor is used for the TEMP monitor function by monitoring its voltage over temperature. The temperature dependence of this diode voltage can be understood in the equation: $V_D = nV_T \ln(\frac{I_D}{I_S})$

where V_T is the thermal voltage (kT/q), and n, the ideality factor, is 1 for the diode connected PNP transistor being used in the YPM04644. I_S is expressed by the typical empirical equation: $I_S = I_0 e^{(\frac{-V_{G0}}{V_T})}$

where I_0 is a process and geometry dependent current, (I_0 is typically around 20k orders of magnitude larger than I_S at room temperature) and V_{G0} is the band gap voltage of 1.2V extrapolated to absolute zero or -273°C.

If we take the IS equation and substitute into the V_D equation, then we get: $V_D = V_{G0} - (\frac{kT}{q}) \ln(\frac{I_0}{I_D}), V_T = \frac{kT}{q}$

The expression shows that the diode voltage decreases (linearly if I_0 were constant) with increasing temperature and constant diode current. Figure 6 shows a plot of V_D vs Temperature over the operating temperature range of the YPM04644.

If we take this equation and differentiate it with respect to temperature T, then: $\frac{dV_D}{dT} = -\frac{V_{G0}-V_D}{T}$。

This dV_D/dT term is the temperature coefficient equal to about -2mV/K or -2mV/℃. The equation is simplified for the first order derivation.

Solving for T, $T = -(V_{G0}-V_D)/(dV_D/dT)$ provides the temperature.

1st Example: Figure 7 for 27℃, or 300K the diode voltage is 0.598V, thus, 300K=-(1200mV-598mV)/- 2.0mV/K)
2nd Example: Figure 7 for 75℃, or 350K the diode voltage is 0.50V, thus, 350K=-(1200mV-500mV)/-2.0mV/K)
Converting the Kelvin scale to Celsius is simply taking the Kelvin temp and subtracting 273 from it.
A typical forward voltage is given in the electrical characteristics section of the data sheet, and Figure 7 is the plot of this forward voltage. Measure this forward voltage at 27℃ to establish a reference point. Then using the above expression while measuring the forward voltage over temperature will provide a general temperature monitor.
Connect a resistor between TEMP and V_{IN} to set the current to 100μA.

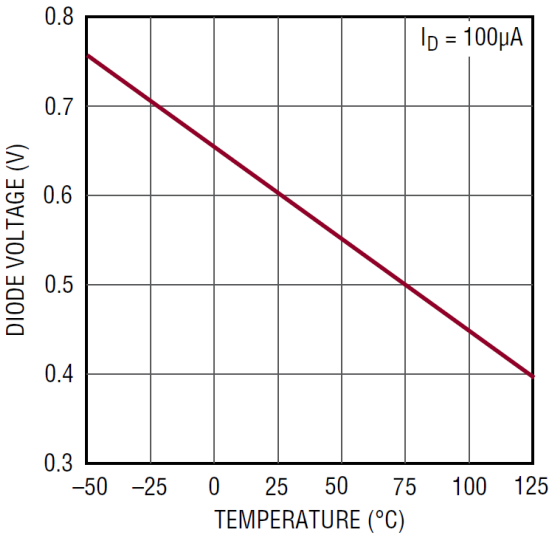


Figure 7. Diode Voltage V_D vs Temperature T(°C)

Thermal Considerations and Output Current Derating
The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD 51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a Module package mounted to a hardware test board: defined by JESD 51-9 (“Test Boards for Area Array Surface Mount Package Thermal Measurements”)
The motivation for providing these thermal coefficients in found in JESD 51-12 (“Guidelines for Reporting and Using Electronic Package Thermal Information”).
Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to predict the Module regulator’s thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided in this data sheet can be used in a manner that yields insight and guidance pertaining to one’s application-usage, and can be adapted to correlate thermal performance to one’s own application.
The Pin Configuration section typically gives four thermal coefficients explicitly defined in JESD 51-12; these coefficients are quoted or paraphrased below:
θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as “still air” although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.
$\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the page. In the typical Module regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don’t generally match the user’s application.
θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical Module regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don’t generally match the user’s application.
θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the Module regulator and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board

temperature is measured a specified distance from the package.

A graphical representation of the aforementioned thermal resistances is given in Figure 8; blue resistances are contained within the Module regulator, whereas green resistances are external to the Module package.

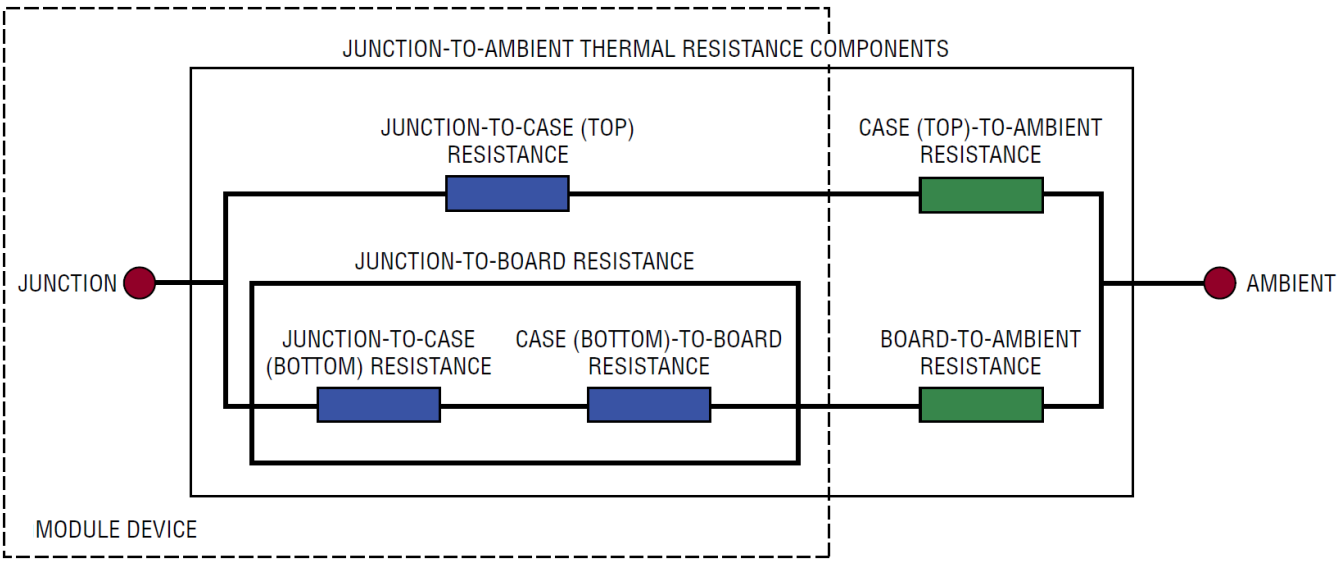


Figure 8. Graphical Representation of JESD 51-12 Thermal Coefficients

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD 51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a Module regulator. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the Module package—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively.

In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within the YPM04644, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the YPM04644 and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD 51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the YPM04644 with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. An outcome of this process and due diligence yields the set of derating curves shown in this data sheet.

Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above junction temperature multiplicative factor. The printed circuit board is a 1.6mm thick four-layer board with two-ounce copper for the two outer layers and one ounce copper for the two inner layers. The PCB dimensions are 95mm × 76mm.

The 20A represents all four channels in parallel at 5A each. The four parallel channels have their currents reduced at the same rate to develop an equivalent θ_{JA} circuit evaluation with thermal couples or IR camera used to validate the thermal resistance values.

Safety Considerations

The YPM04644/YPM4644E modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support thermal shutdown and overcurrent protection.

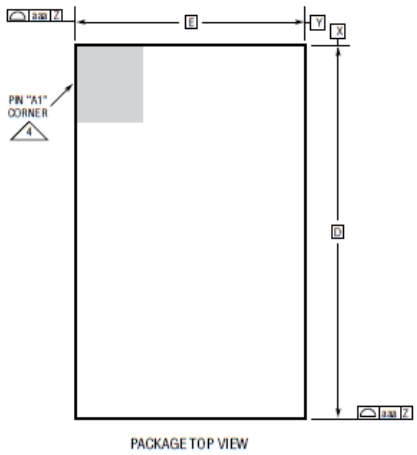
PCB Layout Check List

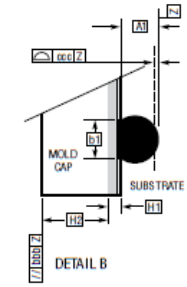
The high integration of YPM04644/YPM04644E makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

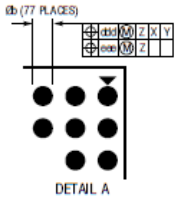
1) Use large PCB copper areas for high current paths, including V_{IN1} to V_{IN4}, GND, V_{OUT1} to V_{OUT4}. It helps to minimize the PCB conduction loss and thermal stress.
2) Place high frequency ceramic input and output capacitors next to the V_{IN}, GND and V_{OUT} pins to minimize high frequency noise.
3) Place a dedicated power ground layer underneath the unit.
4) To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
5) Do not put via directly on the pad, unless they are capped or plated over.
6) Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
7) For parallel modules, tie the V_{OUT}, V_{FB}, and COMP pins together. Use an internal layer to closely connect these pins together. The TRACK/SS pin can be tied a common capacitor for regulator soft-start.
8) Bring out test points on the signal pins for monitoring.

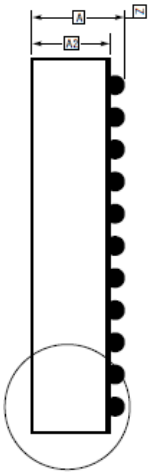
Package Information

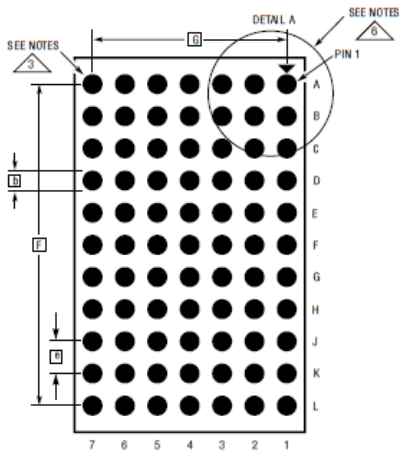
BGA Package
77-Lead (15.00mm × 9.00mm × 5.01mm)
(Reference LTC DWG# 05-08-1900 Rev E)

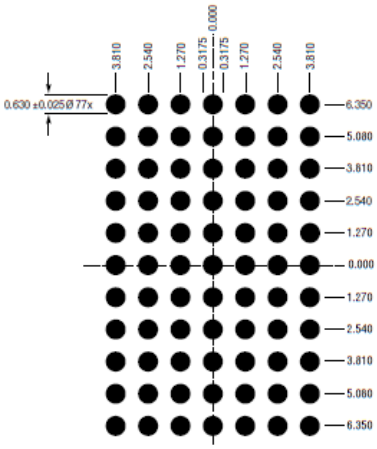






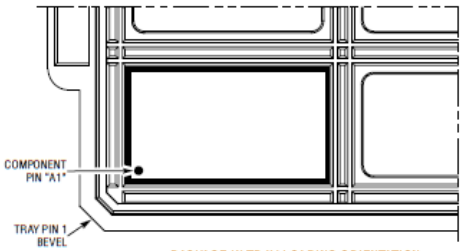






DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.81	5.01	5.21	
A1	0.50	0.60	0.70	BALL HT
A2	4.31	4.41	4.51	
b	0.60	0.75	0.90	BALL DIMENSION
b1	0.60	0.63	0.66	PAD DIMENSION
D		15.00		
E		9.00		
e		1.27		
F		12.70		
G		7.62		
H1	0.36	0.41	0.46	SUBSTRATE THK
H2	3.95	4.00	4.05	MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 77				

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JESD MS-028 AND JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



IMPORTANT NOTICE AND DISCLAIMER

YuanyiMicro provides technical and reliability data(including datasheets), design resource(including reference designs), application and other design material, web tools, safety information, and other resources “AS IS” and with all faults, and disclaims all warranties, express and implied, including without limitation any implied warranties of merchantability, fitness for a particular purpose or non-infringement of third party intellectual property rights.

These resources are intended for skilled developers designing with YuanyiMicro products. You are solely responsible for

(1) selecting the appropriate YuanyiMicro products for your application,

(2) designing, validating and testing your application, and

(3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. YuanyiMicro grants you permission to use these resources only for development of an application that uses the YuanyiMicro products described in the resource. Other reproduction and display of these resources are prohibited. No license is granted to any other YuanyiMicro intellectual property right or to any third party intellectual property right. YuanyiMicro disclaims responsibility for, and you fully indemnify YuanyiMicro and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

YuanyiMicro products are provided subject to YuanyiMicro Terms of Sale, or other applicable terms provided in conjunction with such YuanyiMicro products.

YunyiMicro provision of these resources does not expand or otherwise alter YuanyiMicro applicable warranties or warranty disclaimers for YuanyiMicro products.

Unless YuanyiMicro explicitly designates a product as custom or customer-specified, YuanyiMicro products are standard, catalog, general purpose devices.

YuanyiMicro objects to and rejects any additional or different terms you may propose.

重要声明和免责声明

源易微“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用源易微产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：

(1) 针对您的应用选择合适的源易微产品，

(2) 设计、验证并测试您的应用，

(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。源易微授权您仅可将这些资源用于研发本资源所述的源易微产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他源易微知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对源易微及其代表造成的任何索赔、损害、成本、损失和债务，源易微对此概不负责。

源易微提供的产品受源易微的销售条款或源易微产品随附的其他适用条款的约束。源易微提供这些资源并不会扩展或以其他方式更改源易微针对源易微产品发布的适用的担保或担保免责声明。

源易微反对并拒绝您可能提出的任何其他或不同的条款。